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CST 334

Lab 4 Write Up

The implementation involves simulating a cache with different cache sizes to analyze the hit rates and miss rates for various memory sizes. The implementation was divided into the following steps:

1. Reading the access patterns: Read the provided "accesses.txt" test file to obtain the sequence of memory accesses.

2. Cache initialization: Initialize the cache with a specified cache size. Values of 10-1500 were selected. Screenshot provided with sample runs, and full .xlsx file included in submission for all values between 10 & 1500.

3. Page replacement algorithm: Implement a FIFO page replacement algorithm to manage the cache and handle page faults.

4. Access simulation: Iterate through the sequence of memory accesses obtained from the test file. For each memory access, check if the page is present in the cache. If it is, count it as a hit. Otherwise, count it as a miss and perform the necessary page replacement operations.

5. Calculate hit rate and miss rate: Based on the total requests, total faults, and hit count, calculate the hit rate and miss rate for each cache size.

6. Plotting the results: Generate a graph to visualize the hit rates for different cache sizes. The x-axis represents the cache size, and the y-axis represents the hit rate and miss rate percentages.

Based on the provided result set, the miss rates for different cache sizes are as follows (generalized sample set – full data set on separate file submission):

Cache Size: 10 - Miss Rate: 99.16%

Cache Size: 48 - Miss Rate: 95.37%

Cache Size: 396 - Miss Rate: 61.56%

Cache Size: 514 - Miss Rate: 50.18%

Cache Size: 783 - Miss Rate: 26.43%

Cache Size: 884 - Miss Rate: 17.68%

Cache Size: 1057 - Miss Rate: 9.99%

Cache Size: 1209 - Miss Rate: 9.99%

Cache Size: 1403 - Miss Rate: 9.99%

Cache Size: 1500 - Miss Rate: 9.99%

Note: The miss rate represents the percentage of memory accesses that resulted in page faults (cache misses). As the cache size increases, the miss rate generally decreases, indicating a higher hit rate and better cache performance. This trend can be observed in the provided results as the cache size increases from 10 to 1500 pages.

*Cache size increases along the x-axis*